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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/613,749	07/11/2000	Satoshi Suzuki	400762/AOYAMA	1153

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/613,749	SUZUKI ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *18-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' amendment filed on January 28, 2003 has been entered on February 04, 2003.

Therefore claim 18 as amended by the amendment and claims 19 to 25 as previously recited as currently pending in the Application.

Claim Rejections - 35 USC § 112

Applicants' on page 3 of their response paragraph 3 contend, " The compound semiconductor substrate is described in the patent application and in the first paragraph of claim 18 as being "electrically isotropic in two mutually orthogonal directions". The exemplary substrate material described in the patent application is gallium arsenide and persons of skill in the art recognize that that material is electrically isotropic in two mutually orthogonal directions. Those persons also recognize that this property and this description of the property means that gallium arsenide is, in many characteristics, anisotropic."

The above contention is not persuasive because Merriam – Webster's Collegiate Dictionary (10 Edn.) defines

ANISOTROPIC : exhibiting properties with **DIFFERENT** values when measured in different directions. (emphasis supplied) (page 46)

ISPTROPIC : exhibiting properties (as velocity of light transmission) with the **SAME** value when measured along axes in all directions. (emphasis supplied) (page 622) .

Therefore it is clear that An isotropic and Isotropic mean opposite things, namely Different values in different directions and Same values in different directions.

Therefore a person of ordinary skill in the art would understand the recited Gallium arsenide compound semiconductor exhibiting electrically isotropic in two mutually orthogonal directions CAN NOT be recognized from this description as having " an isotropic " electrical characteristics.

Applicants' can not mean some other characteristic because those unspecified other characteristics are also not mentioned in the specification as originally filed, where in only electrical characteristics are mentioned.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18 –25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsui (U.S. Patent No. 5,295,901 herein after Tsutsui) in view of Tozawa (Japanese Patent Publication No. 43270024, herein after Tozawa) **OR** Kobayashi (Japanese Patent Publication No. 61-232682 herein after Kobayashi), the previous rejection is reproduced below for the sake of ready reference . (For response to Applicants' arguments see below).

With respect to claim 18, a semiconductor device including , (Tsutsui abstract line 4) a compound semiconductor substrate (Tsutsui Abstract line 1) having a first surface and a second surface.

Tsutsui does not specifically describe the compound semiconductor substrate being electrically isotropic in two mutually orthogonal directions.

However, Taguchi , a patent from the same field of endeavor, describes in col. 2 lines 10-12 the compound semiconductor substrate being electrically isotropic in two mutually orthogonal directions to reduce the alloying of the metal alloy electrode with the substrate GaAs or other compound semiconductor substrate material during high temperature processing thus the electrical resistance of the wiring is reduced to almost zero and allowing the signals to reach its destination without delay or degradation of the signal.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Taguchi's the compound semiconductor substrate being electrically isotropic in two mutually orthogonal directions in Tsutsui's device to reduce the alloying of the metal alloy electrode with the substrate GaAs or other compound semiconductor substrate material during high temperature processing thus the electrical resistance of the wiring is reduced to almost zero and allowing the signals to reach its destination without delay or degradation of the signal. (Taguchi col. 3).

The remaining limitations of claim 18 are :

First second and third active regions on the first surface of the substrate (Tsutsui fig. 1), the first and second active regions being separated by a first insulating region (

Tsutsui col. 4 lines 30-34) and the second and third active regions being separated by a second insulating region. (Tsutsui fig. 1) , a first semiconductor element including first ,second and third channel regions serially connected .

Tsutsui and Taguchi do not specifically describe or teach adjacent channel regions having width directions essentially perpendicular to each other.

However, Tozawa or Kobayashi (English Abstract) , each a patent from the same field of endeavor, describes in its figures adjacent channel regions having width directions essentially perpendicular to each other to improve integration and reduce the size of the devices.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Tozawa's and/or Kobayshi's adjacent channel regions having width directions essentially perpendicular to each other to improve integration and reduce the size of the devices.

(Tozawa figures and /or Kobayashi's English Abstract), a first source electrode and a first drain electrode, adjacent to the first, second and third channel regions and opposing each other with the first, second and third channel regions there between and in ohmic contact with the first, second and third channel. (Tozawa figures), a first gate electrode disposed on the first, second and third active regions and along the first source electrode and the first drain electrode, and bent at first and second bending positions (Tozawa figs. 1 # 1,2 or 3 on the channels and along source electrode 3 and drain electrode 1), a second semiconductor element on the first, second and third active region adjacent to the first semiconductor element (Tozawa fig. 1 LHS (left hand side)

element of 1A), fourth , fifth and sixth channel regions serially connected , adjacent channel regions having width directions essentially perpendicular to each other , the fourth, fifth and sixth channel regions being adjacent to first, second and third channel regions, respectively with one of the first source electrode and the first drain electrode there between (Tozowa fig. 1A), a second source electrode and a second drain electrode in ohmic contact with the first, second and third active regions one of the second source electrode and the second drain electrode and opposing the first drain electrode and opposing the first drain electrode or the first source electrode across the fourth , fifth and sixth channel regions (Tozowa fig. 1 A) and a second gate electrode on the fourth, fifth and sixth channel regions and along one of the second source electrode and a second source electrode, and bent at third and fourth bending positions, wherein the first and second insulating regions are under the first and third bending portions of the first and second gate electrodes and under the second and fourth bending positions of the first and second gate electrodes respectively. (Tozawa fig. 1A, electrodes 1 and 3 and regions between the electrodes that is insulating regions).

With respect to claim 19, wherein the first source electrode is connected to a conductive film on the second surface of the semiconductor substrate through a via-hole in the first source electrode (Tozawa fig. 1a # 3 connected to bottom portion (eg. 2a) through via hole and interconnection part # A in fig. 1b).

With respect to claim 20, wherein the first bending position of the first gate electrode and the third bending position of the second gate electrode lie on a straight

line substantially parallel to a longer side of the first, second and third active regions. (Tsutsui fig. 7 and Tozawa fig. 1a).

With respect to claim 21, wherein the first gate electrode is bent in opposite directions at the first and second bending positions and wherein the second gate electrode extends substantially at a n uniform spacing from the first gate electrode. (Tsutsi fig. 7 and Tozawa fig. 1a).

With respect to claim 22, wherein the first gate electrode and second gate electrode share one of the first source and drain electrode (previous i.e. cancelled claim 11, Tozawa fig. 1a).

With respect to claim 23, wherein the first gate electrode is bent at right angles at each of the first and second bending positions . (previous i.e. cancelled claim 12, Tozawa fig. 1a).

With respect to claim 24 wherein the second gate electrode is bent at right angles at each of the third and fourth bending positions . (previous i.e. cancelled claim 12, Tozawa fig. 1a).

With respect to claim 25 wherein an angle between the width direction of the first gate electrode and a longer side of the first, second and third active regions is essentially 45^{0}. (previous i.e. cancelled claim 13 , Tozawa fig. 1a) .

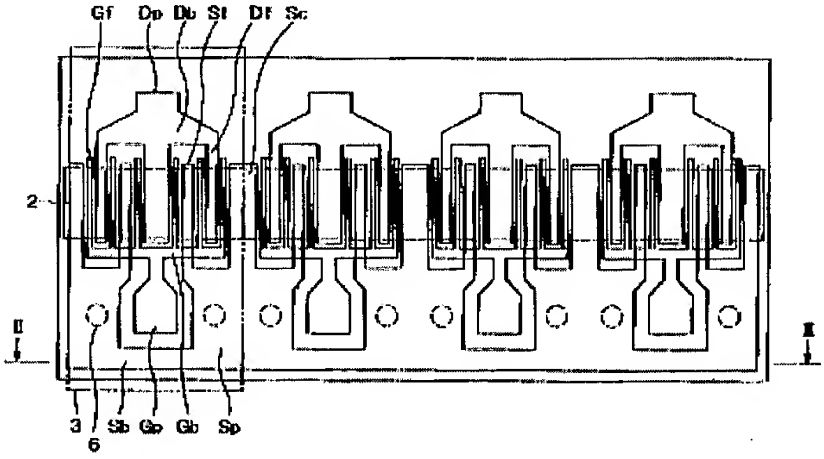
Response to Arguments

Applicant's arguments filed 01/28/03 have been fully considered but they are not persuasive. for the following reasons :

Applicants' first argument is that the applied Tsutsui reference in fig. 1a etc . shows only a single active region 2.

Tsutsui fig. 1 is reproduced below :

FIG. 1
(PRIOR ART)



and the description of figure 1 includes col. 1 lines 13 to 26 (reproduced below)

FIG. 1 is a plan view of the conventional high-power GaAs FET provided with a PHS (plated heat sink) of a gold plated layer on the back surface of the conventional GaAs substrate, and FIG. 2 is a section taken along line II—II of FIG. 1. In the shown high-power GaAs FET, a FET chip is formed with four unit cells 3 (shown by surrounding with two dotted lines) arranged in parallel. The unit cell 3 has a gate electrode, a drain electrode and a source electrode. These electrodes are comb-shaped configuration with finger-shaped gate electrode Gf, finger-shaped drain electrode Df and finger-shaped source electrode Sf, on an active region 2 formed in the surface portion of the substrate by ion implantation. Adjacent cells are connected by connecting respective source electrodes Sc to each other.

Therefore the above figure shows at least four unit cells each having at least one active regions for a total of at least four (4) active regions.

Further ,Tsutsui in col. 3 lines 48-66 states :

FIG. 7 is a plan view of the first embodiment of a FET chip according to the present invention, and FIG. 8 is a section taken along line VIII—VIII of FIG. 7.

In the shown embodiment, finger-shaped gate electrodes Gf are formed selectively covering an active region 2 on one primary surface portion of a GaAs substrate. At opposite sides of the finger-shaped gate electrodes Gf, finger-shaped source electrodes Sf and finger-shaped drain electrodes Df are formed selectively covering the active region 2 of the GaAs substrate.

Six sets of FETs respectively constituted of the finger-shaped gate electrode Gf, the finger-shaped source electrode Sf and the finger-shaped drain electrode Df, are arranged in parallel relationship to form each individual unit cell 3. In each unit cell 3, adjacent finger-shaped gate electrodes Gf are arranged to have the finger-shaped source electrode Sf or the finger-shaped drain electrode Df in common. In the

Therefore Tsutsui figure 1 shows plural active regions similar to regions 16 of at least figures 1 to 4 of the instant application.

Therefore the comparision of Tsutsui to the instant application is not flawed.

As Tsutusi shows similar multiple active regions (as stated above) it also shows first and second insulating regions that separate respective parts of the first, second and third active regions. (as previously stated Tsutsui in col.4 lines 30 to 37, reproduced below)

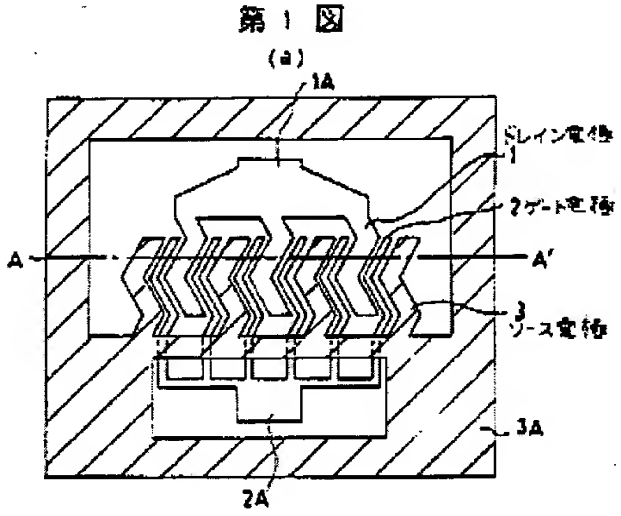
The active region 2 is surrounded by an insulation region formed by ion implantation. A part of surface of the insulation region and the active region is covered with a SiO_2 layer 4. The finger-shaped source electrode Sf and the finger-shaped drain region Df are connected with the active region through a contact hole portion (not shown) provided through the SiO_2 layer 4.

Therefore the statement in the Official Action finds Full and complete support in the prior art and therefore for a second reason the comparison is correct and therefore the rejection based on the comparison is similarly correct.

Applicants' next contention that, " Tozawa fig. 1 A, electrodes 1 and 3 and regions between the electrodes " are the insulating regions of the final paragraph of claim 18. This comparison is incorrect on three independent grounds " is not persuasive for the following reasons.

First claim 18 refers to the bending portions of the gate electrodes. The electrodes 1 and 3 in Tozawa are source and rain electrodes, not gate electrodes. Thus the comparison is inappropriate."

Tozawa figure 1 A is reproduced below .



Elements 2 are gate electrodes.

Therefore the comparison is appropriate.

Applicants' second independent ground , " Second, what the regions in Tozawa between the source and drain electrodes 1 and 3, regions including the gate electrodes 2, might be, is not disclosed by Tozawa. Assuming there is electrical insulation in those regions, the claim limitation is still not meet. Claim 18, as examined and as pending

here refers to the first and second insulating regions as being under the bending portions of the first and second gate electrodes, not between. This difference is important and demonstrates a further error in the rejection."

It is noted that Figure 1 A is a cross sectional view and not a top view and one cannot conclude from a cross sectional view that the insulation layer is not below the first and second gate electrodes, further if the first and second gate electrodes were not insulated the gates upon contacting each other (without the insulation there between) would produce an electrical shot and the device would be inoperable.

Therefore the difference as alleged between Tozawa and the presently recited claim18 does not exist and therefore there is no error in the rejection.

Applicants' third independent ground, " Third, of course, since neither Tsutsui nor Tozawa describes multiple active regions, pairs of which are separated by respective insulating regions, it would be impossible for any combination of those references to include all of the references to include all of the elements of the final paragraph of claim 18 anyway. Based upon any of these grounds, the rejection is as erroneous with respect to its assertion that the elements of the final paragraph of claim 18 are found in the prior art."

As stated above Tsutsui describes and its figures show multiple active regions in figures 1 & 7 and col. 1lines 12-26 and col. 3 lines 48-67.

Therefore all of the presently recited elements of claim 18 are described and /or suggested by the applied prior art of record.

Applicants' content that dependent claims 19 to 25 are allowable because they depend upon allegedly allowable claim 18.

However as shown above claim 18 is not allowable, therefore dependent claims 19 to 25 are also not allowable and rejected for reasons stated above.

As the same references that were used before are also used herein this forms a separate basis for making this action Final.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7722.

Steven H. Rao

Patent Examiner

March 28, 2003.

LONG PHAM
PRIMARY EXAMINER